

COS/MOS INTEGRATED CIRCUIT

4094B

HCC/HCF 4094B

8-STAGE SHIFT-AND-STORE BUS REGISTER

- 3-STATE PARALLEL OUTPUTS FOR CONNECTION TO COMMON BUS
- SEPARATE SERIAL OUTPUTS SYNCHRONOUS TO BOTH POSITIVE AND NEGATIVE CLOCK EDGES FOR CASCADING
- MEDIUM SPEED OPERATION - 5 MHz AT 10V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The **HCC 4094B** (extended temperature range) and **HCF 4094B** (intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in-line plastic or ceramic package, ceramic flat package and plastic micropackage.

The **HCC/HCF 4094B** is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high. Two serial outputs are available for cascading a number of **HCC/HCF 4094B** devices. Data is available at the Q_S serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q'_S terminal on the next negative clock edge, provides a means for cascading **HCC/HCF 4094B** devices when the clock rise time is slow.

ABSOLUTE MAXIMUM RATINGS

V_{DD}^*	Supply voltage: HCC types HCF types	-0.5 to 20	V
V_i	Input voltage	-0.5 to 18	V
I_i	DC input current (any one input)	-0.5 to $V_{DD} + 0.5$	V
P_{tot}	Total power dissipation (per package)	± 10	mA
	Dissipation per output transistor for T_{op} = full package-temperature range	200	mW
T_{op}	Operating temperature: HCC types HCF types	100	mW
		-55 to 125	°C
T_{stg}	Storage temperature	-40 to 85	°C
		-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

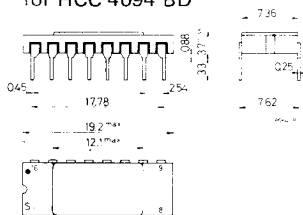
ORDERING NUMBERS:

HCC 4094 BD for dual in-line ceramic package
HCC 4094 BF for dual in-line ceramic package, frit seal
HCC 4094 BK for ceramic flat package
HCF 4094 BE for dual in-line plastic package
HCF 4094 BF for dual in-line ceramic package, frit seal
HCF 4094 BM for plastic micropackage

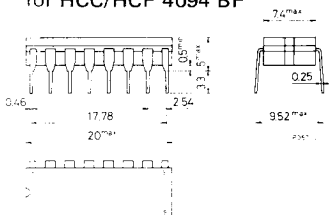
HCC/HCF 4094B

MECHANICAL DATA(dimensions in mm)

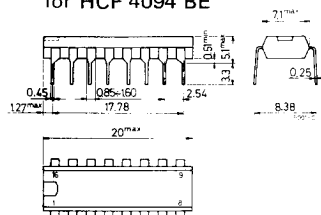
Dual in-line ceramic package
for HCC 4094 BD



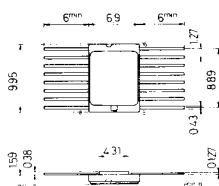
Dual in-line ceramic package
for HCC/HCF 4094 BF



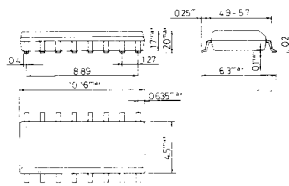
Dual in-line plastic package
for HCF 4094 BE



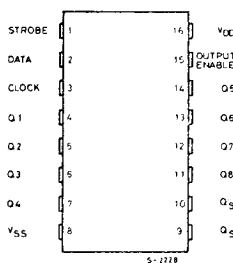
Ceramic flat package for
HCC 4094 BK



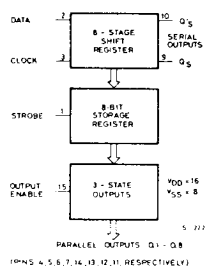
Plastic micropackage for
HCF 4094 BM



CONNECTION DIAGRAM



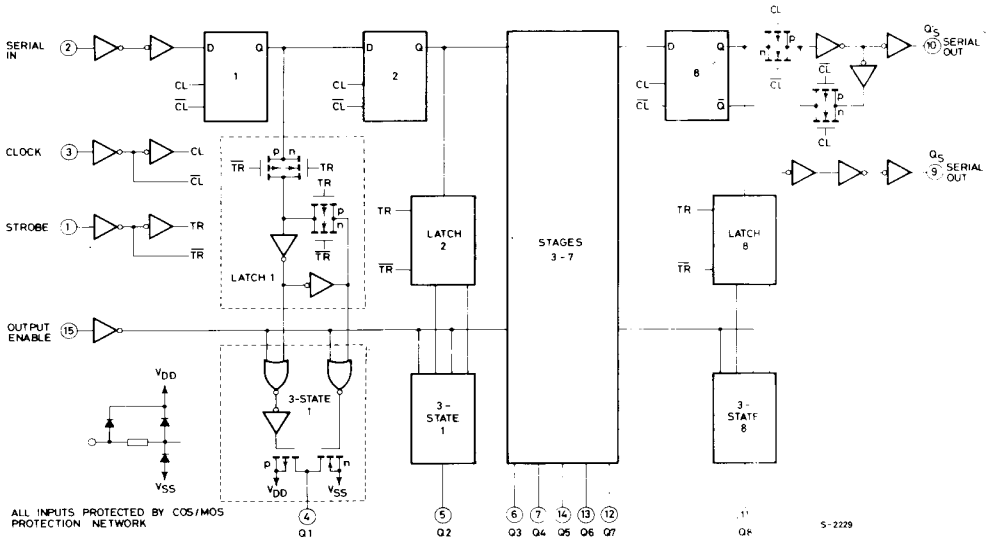
FUNCTIONAL DIAGRAM



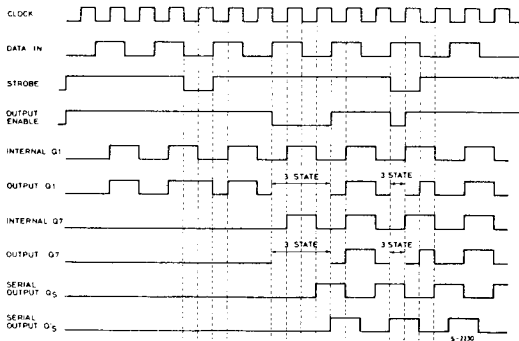
RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: HCC types	3 to 18	V
	HCF types	3 to 15	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: HCC types	-55 to 125	°C
	HCF types	-40 to 85	°C

LOGIC DIAGRAM



TIMING DIAGRAM



TRUTH TABLE

CL [▲]	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	Q _N	Q _S [*]	Q' _S
↗	0	X	X	OC	OC	Q7	NC
↘	0	X	X	OC	OC	NC	Q7
↗	1	0	X	NC	NC	Q7	NC
↘	1	1	0	0	Q _{N-1}	Q7	NC
↗	1	1	1	1	Q _{N-1}	Q7	NC
↘	1	1	1	NC	NC	NC	Q7

▲ = Level Change

X = Don't Care

NC = No Change

OC = Open Circuit

*At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the Q_S output.

Logic 1 ≡ High

Logic 0 ≡ Low

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V _I (V)	V _O (V)	I _O (μ A)	V _{DD} (V)	T _{Low} *		25°C			T _{High} *		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I _L	Quiescent current	HCC types	0/ 5			5		5		0.04	5		150	μ A
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
		0/15			15		80		0.04	80		600		
V _{OH}	Output high voltage	0/ 5		< 1	5	4.95		4.95				4.95		V
		0/10		< 1	10	9.95		9.95				9.95		
		0/15		< 1	15	14.95		14.95				14.95		
V _{OL}	Output low voltage	5/0		< 1	5		0.05			0.05		0.05		V
		10/0		< 1	10		0.05			0.05		0.05		
		15/0		< 1	15		0.05			0.05		0.05		
V _{IH}	Input high voltage		0.5/4.5	< 1	5	3.5		3.5				3.5		V
			1/9	< 1	10	7		7				7		
			1.5/13.5	< 1	15	11		11				11		
V _{IL}	Input low voltage		4.5/0.5	< 1	5		1.5			1.5		1.5		V
			9/1	< 1	10		3			3		3		
			13.5/1.5	< 1	15		4			4		4		
I _{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I _{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I _{IH} , I _{IL}	Input leakage current	HCC types	0/18	Any input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μ A
		HCF types	0/15			15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1	
I _{OH} , I _{OL}	3-state output leakage current	HCC types	0/18	0/18		18		± 0.4		$\pm 10^{-4}$	± 0.4		± 12	μ A
		HCF types	0/15	0/15		15		± 1.0		$\pm 10^{-4}$	± 1.0		± 7.5	
C _I	Input capacitance				Any input					5	7.5			pF

* T_{Low} = - 55°C for HCC device; -40°C for HCF device.* T_{High} = +125°C for HCC device; +85°C for HCF device.

The Noise Margin for both "1" and "0" level is:

1V min. with V_{DD}= 5V

2V min. with V_{DD}= 10V

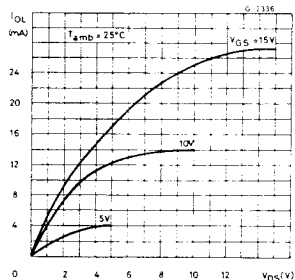
2.5V min. with V_{DD}= 15V

DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$, typical temperature coefficient for all $V_{DD} = 0.3\%/^{\circ}\text{C}$ values, all input rise and fall time = 20 ns)

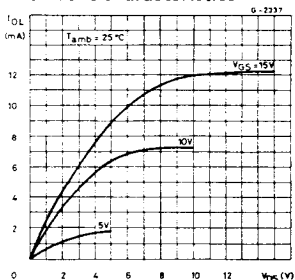
Parameter		Test conditions	Values			Unit
			V _{DD} (V)	Min.	Typ.	
t _{PLH} , t _{PHL}	Propagation dealy time Clock to serial output Q _S	5		300	600	ns
		10		125	250	
		15		95	190	
t _{PLH} , t _{PHL}	Propagation delay time Clock to serial output Q' _S	5		230	460	ns
		10		110	220	
		15		75	150	
t _{PLH} , t _{PHL}	Propagation delay time Clock to parallel output	5		420	840	ns
		10		195	390	
		15		135	270	
t _{PLH} , t _{PHL}	Propagation delay time Strobe to parallel output	5		290	580	ns
		10		145	290	
		15		100	200	
t _{PHZ}	Propagation delay time Output enable to parallel output: Output High to High Impedance	5		140	280	ns
		10		75	150	
		15		55	110	
t _{PLZ}	Out Low to High Impedance	5		225	450	ns
		10		95	190	
		15		70	140	
t _W	Strobe pulse width	5	200	100		ns
		10	80	40		
		15	70	35		
t _W	Clock pulse width	5	200	100		ns
		10	100	50		
		15	83	40		
t _{setup}	Data setup time	5	125	60		ns
		10	55	30		
		15	35	20		
t _{TLH} , t _{THL}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
t _r , t _f	Clock input rise or fall time	5	15			μs
		10	5			
		15	5			
f _{max}	Maximum clock input frequency	5	1.25	2.5		MHz
		10	2.5	5		
		15	3	6		

HCC/HCF 4094B

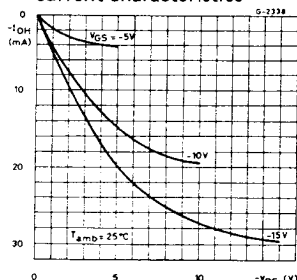
Typical output low (sink) current characteristics



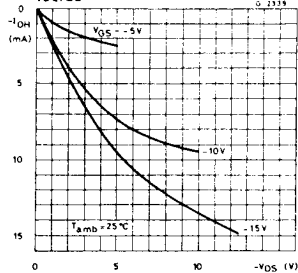
Minimum output low (sink) current characteristics



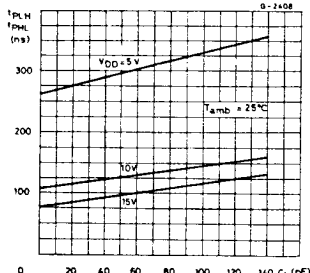
Typical output high (source) current characteristics



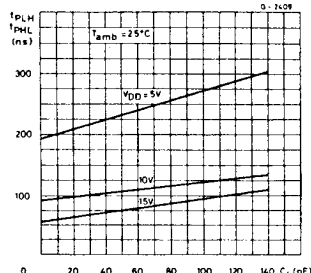
Minimum output high (source) current characteristics



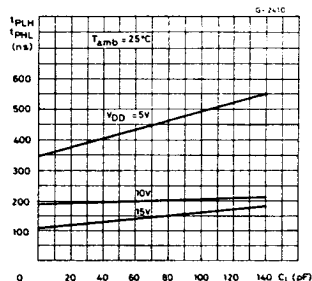
Clock-to-serial output Q_S propagation delay vs. C_L



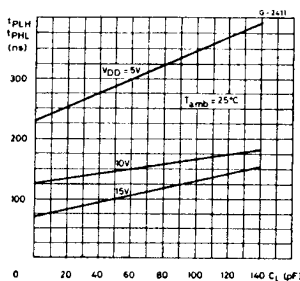
Clock-to-serial output Q'_S propagation delay vs. C_L



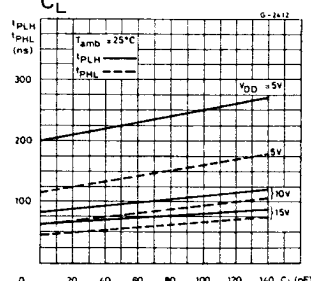
Clock-to-parallel output propagation delay vs. C_L



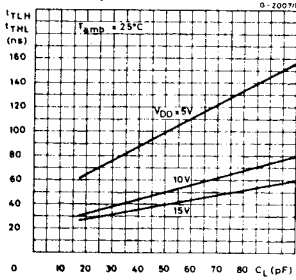
Strobe-to-parallel output propagation delay vs. C_L



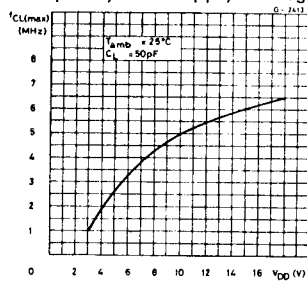
Output enable-to-parallel output propagation delay vs. C_L



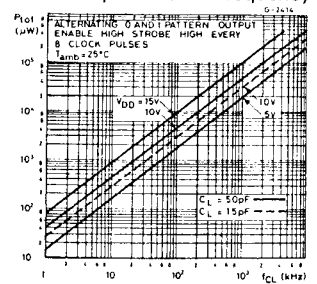
Typical transition time vs. load capacitance



Typical maximum-clock frequency vs. supply voltage

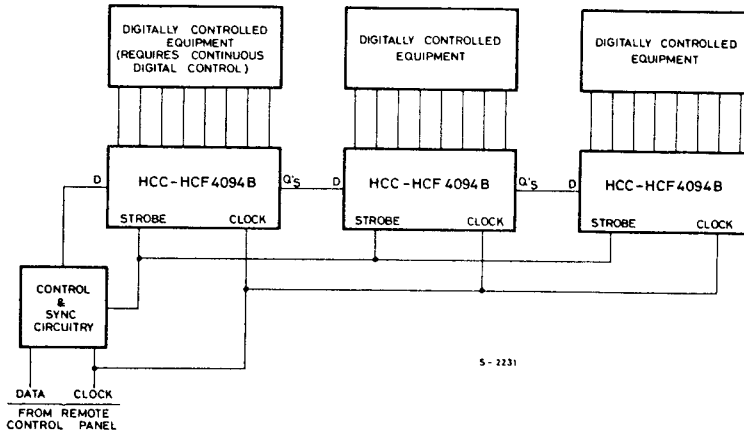


Dynamic power dissipation vs. input clock frequency



TYPICAL APPLICATION

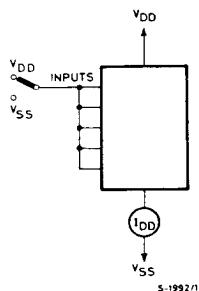
Remote control holding register



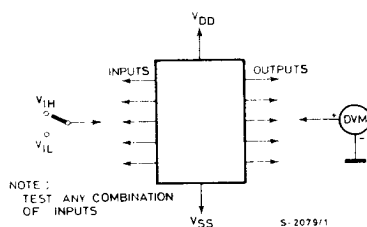
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TEST CIRCUITS

Quiescent device current



Noise immunity



Input leakage current

